AMENDMENTS TO THE SPECIFICATION

Please replace paragraph 34 of page 10 of the specification with the following amended paragraph:

FIG. 7 illustrates a cross-sectional view of an array of microelectronic packages in accordance with another embodiment of the present invention. First microelectronic package 100 includes a first carrier substrate 112 having a die side 118 and a non-die side 119. A die 110 is coupled to die side 118. Die 110 is covered with encapsulation material 114, though encapsulation material 114 is not required. The encapsulation material 114 having a form factor with a peripheral surface 111 opposite of the die 110 that intersects the die side 118 of the carrier substrate 112. Land pads 116 are positioned at or near the die side 118 of carrier substrate 112.

Please replace paragraph 36 of page 11 of the specification with the following amended paragraph:

Intermediate substrate 120 may be disposed between the die side 118 of the first carrier substrate 112 and the non-die side 119' of the second carrier substrate 112' and located external to the peripheral surface 111 of the encapsulation material 114. Conductive risers 115 may be disposed within intermediate substrate 120. The conductive risers 115 may have a first end 122 and a second end 124. The conductive risers may be positioned such that the first ends may electrically couple with the land pads 116 and the second ends may electrically couple with a corresponding bond pads 117 of the adjacent carrier substrate 112'.